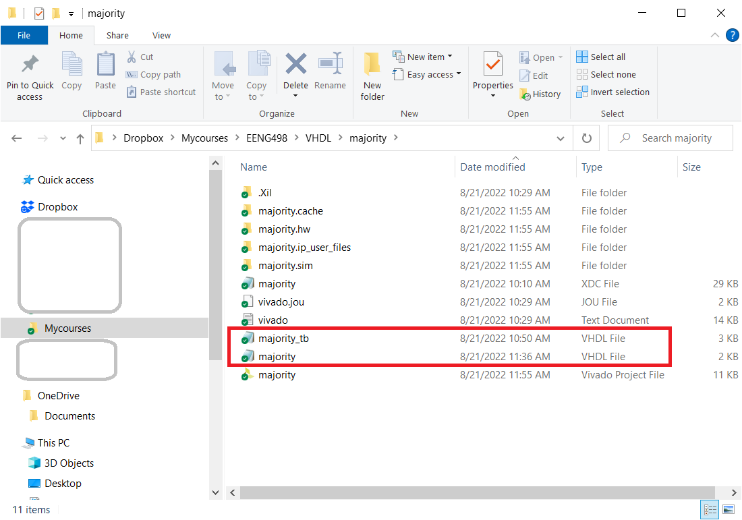
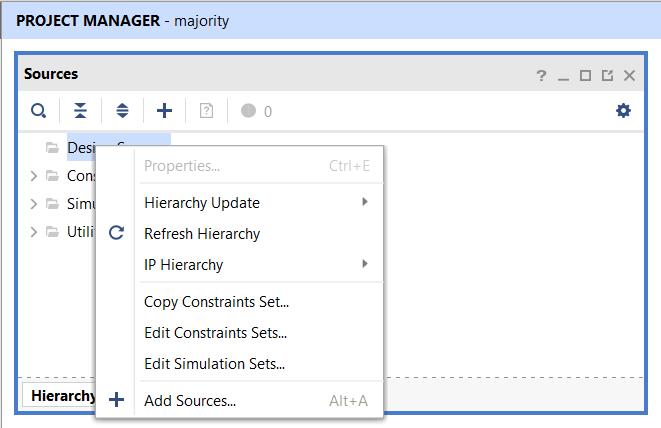
1. Create a project

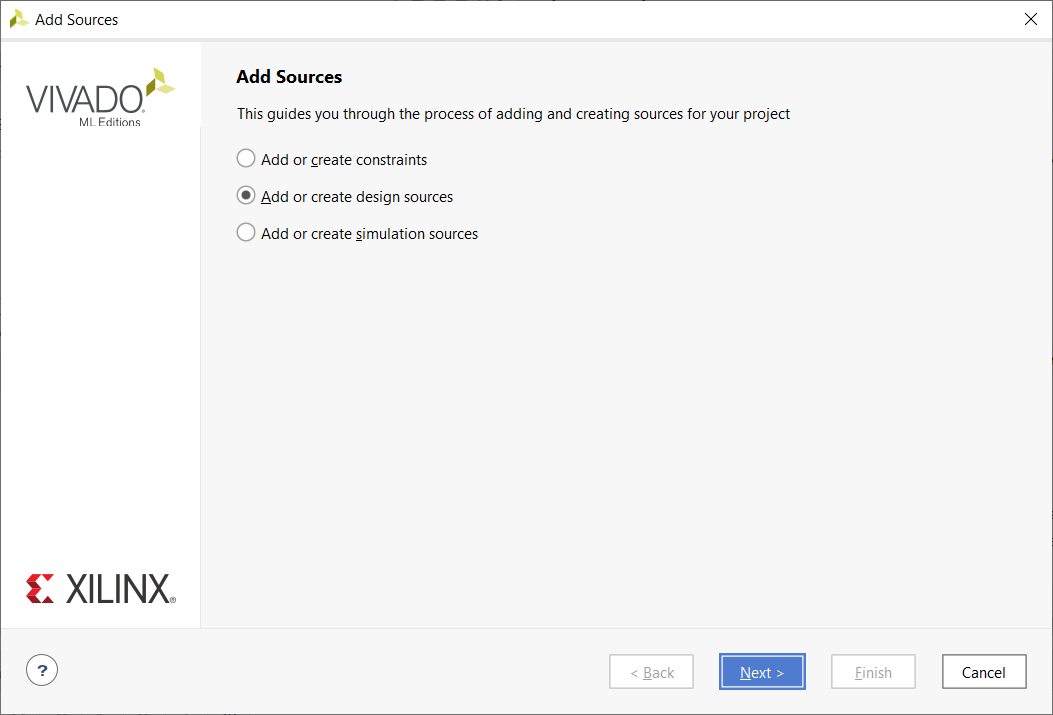
2. Download any source files and testbench files into the project directory.



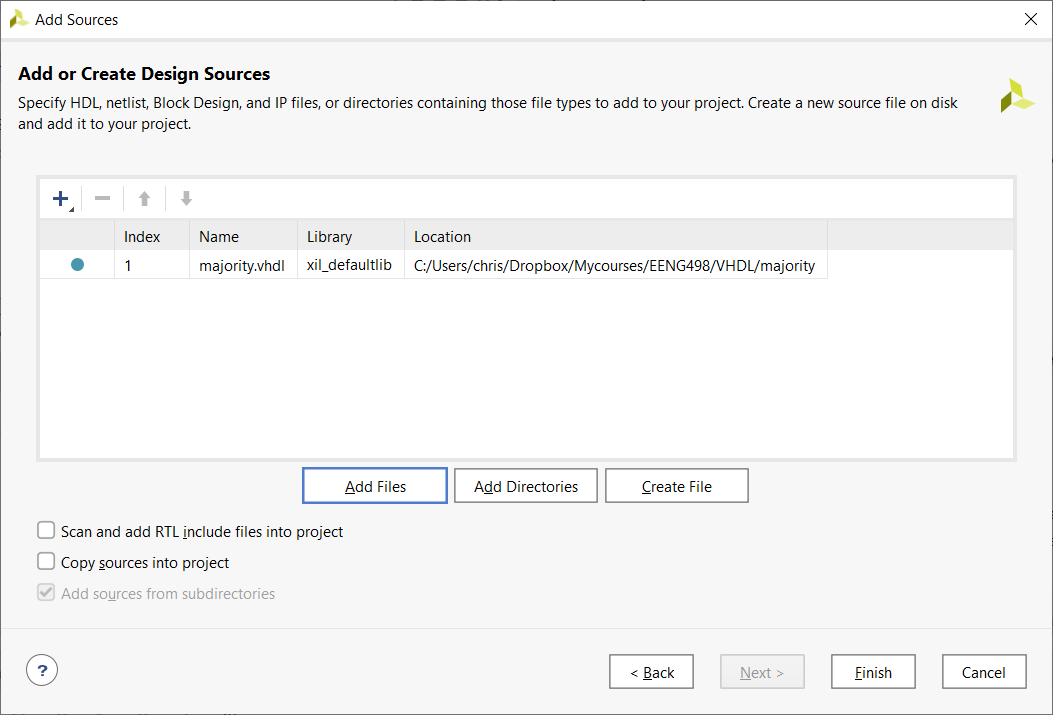
3. In Vivado, In the Sources pane of the Project Manager window, right mouse click on Design Sources folder and select “Add Sources” to launch the Add Sources Wizard.



4. In the Add Sources, leave the default radio button.



5. In the Add or Create Design Sources pop-up, click on “Add Files” and select source files which contain synthesizable VHDL code. Then click Finish.

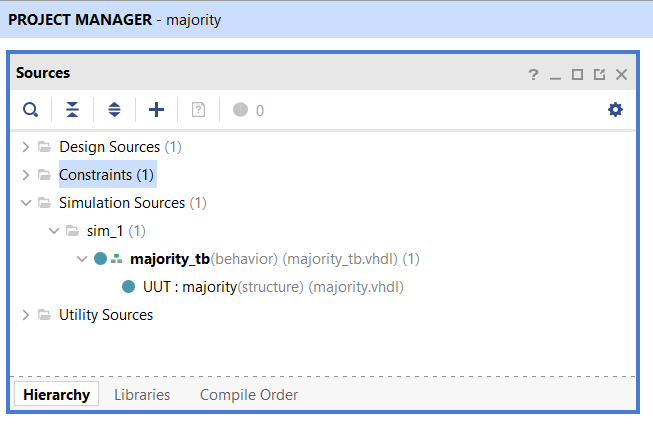


6. Add testbench files to the Simulation Sources folder by right mouse clicking on the Simulation Sources folder in the Sources pane of the Project Manager window. Select “Add Sources” and then follow steps 4 and 5 to add the testbench files.



7. If you have any constraint files, add them by right mouse clicking on the Constraints folder in the Sources pane of the Project Manager window.

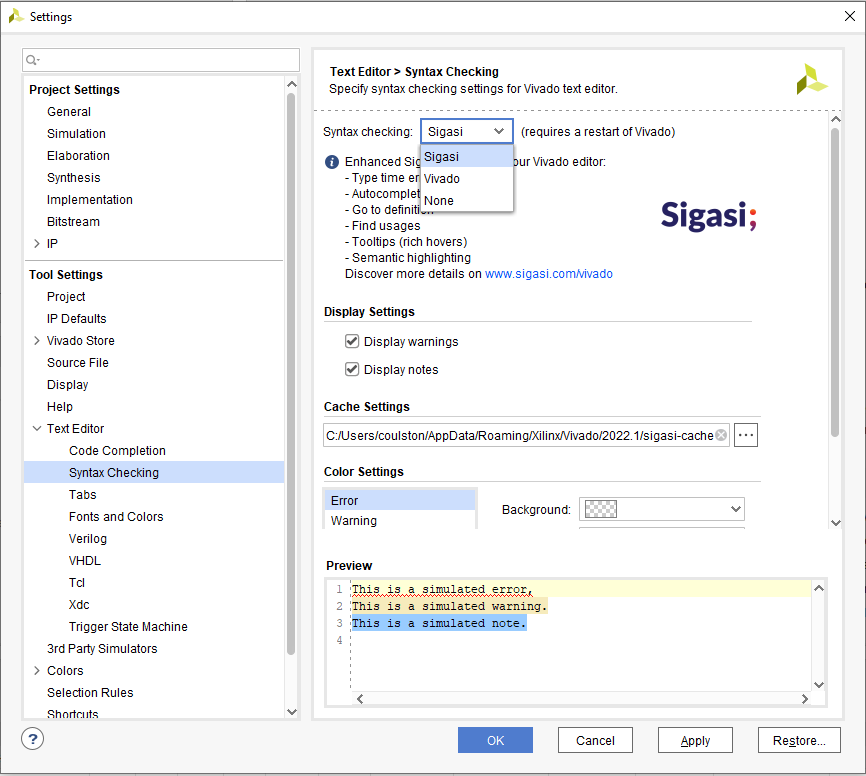
8. When complete, the unit under test (UUT) will be nested inside the testbench.



9. To open a source file, you should double click on the file name in the Sources pane of the Project Manager. The default editor for Vivado, Sigasi, has an annoying habit of crashing whenever you try to open a file. You will know this is happening when you are stuck at the following window for more than 10 seconds.



If this is happening more than you would like, you can change the default editor to Vivado by clicking on Tools -> Settings. In the Settings pop-up, click on Tool Settings -> Text Editor -> Syntax Checking. Then change the Syntax checking pull-down to Vivado. You will need to restart Vivado for this change to take effect.



10. You are ready to perform a simulation to determine if your design file is correct.